

In re Patent Application of:  
**SMYTH ET AL.**  
Serial No. 10/022,595  
Filing Date: **DECEMBER 13, 2001**  
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#### REMARKS

The Examiner is thanked for the thorough examination of the present application. Claims 1-28 have been cancelled without prejudice to Applicants' rights to file a divisional patent application directed to the subject matter thereof. In view of the arguments presented in detail below, it is submitted that all of the claims are patentable.

#### I. The Claimed Invention

The present invention is directed to an electronic module. As recited in independent Claim 29, for example, the electronic module includes a low temperature co-fired ceramic (LTCC) substrate, and at least one capacitive structure embedded in the LTCC substrate. More particularly, the at least one capacitive structure includes a pair of electrode layers, an inner dielectric layer between the pair of electrode layers, and at least one outer dielectric layer adjacent at least one of the electrode layers and opposite the inner dielectric layer. The at least one outer dielectric layer has a dielectric constant less than a dielectric constant of the inner dielectric layer. The electronic module further includes at least one electronic device mounted on the LTCC substrate and electrically connected to the at least one embedded capacitive structure. The electronic module thus provides a relatively high capacitance embedded capacitive structure while also providing adequate space for signal routing, for example.

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## **II. The Claims Are Patentable**

The Examiner rejected independent Claim 29 over Takagi et al. (U.S. Patent No. 4,800,459) in view of Klee et al. (U.S. Patent No. 6,125,027), and also based upon the foreign parent application of Klee et al. (DE 19630883) in view of Alexander (U.S. Patent No. 5,661,882). Since U.S. Patent No. 6,125,027 is based upon the U.S. equivalent of the parent German application DE 19630883, both will be referred to herein as "Klee et al.," and citations provided are to the English language U.S. patent.

### **A. Takagi et al. and Klee et al.**

Takagi et al. is directed to a circuit substrate 1 which includes a ceramic laminated structure 10 having a plurality of ceramic layers 2-7 including ceramic layers 3-6 having cavities 44-49 therein. Chip-like electronic components, such as a laminated ceramic capacitor 26, and a resistor 28 are received in the cavities. The chip-like electronic components are formed with external terminal electrodes 29-34, respectively. Conductors 15-20 are formed in through holes 35-43 provided in the ceramic layers and interfaces between adjacent pairs of the ceramic layers to be connected to the external terminal electrodes. See, e.g., abstract and FIG. 1 of Takagi et al.

The Examiner correctly acknowledges that Takagi et al. fails to teach or fairly suggest at least one capacitive structure comprising a pair of electrode layers, an inner dielectric layer between the pair of electrode layers, and at least one outer dielectric layer adjacent at least one of the

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electrode layers and opposite the inner dielectric layer, where the at least one outer dielectric layer has a dielectric constant less than a dielectric constant of the inner dielectric layer. The Examiner also correctly acknowledges that Takagi et al. fails to teach or fairly suggest at least one electronic device mounted on the LTCC substrate and electrically connected to the at least one embedded capacitive structure.

Nonetheless, the Examiner contends that Klee et al. provides all of the above-noted deficiencies. Klee et al. is directed to a surface-mountable capacitor structure which includes a substrate layer 1 of glass or  $\text{Al}_2\text{O}_3$ , an anti-reaction (or "leveling") Ti layer 2 on the substrate, a first electrode layer 3 on the anti-reaction layer, a dielectric 4 on the first electrode, a second electrode 5 on the dielectric layer, and a protective organic layer 6 over the second electrode layer. See, e.g., FIG. 1, abstract, and col. 7, line 4 through col. 8, line 12 of Klee et al.

The Examiner contends that the Klee et al. capacitive structure is equivalent with the at least one capacitive structure recited in Claim 29. However, the Examiner never states in the Office Action that Klee et al. teaches or fairly suggests mounting an electronic device on an LTCC substrate as recited in Claim 29, which it does not. See page 5 of the Office Action. In fact, the Examiner acknowledges on page 7 of the Office Action that the parent German application (DE 19630883) does not teach or fairly suggest at least one electronic device mounted on the LTCC substrate as in Claim 29. Accordingly, as an initial matter,

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it is respectfully submitted that a proper prima facie case of obviousness has not been established because the proposed combination of references fails to teach or fairly suggest ALL of the claimed recitations.

Moreover, it is also respectfully submitted that the selective combination of Klee et al. with Takagi et al. is improper, as these references teach away from such a selective combination. For example, Takagi et al. teaches that a "chip-like" laminated capacitive structure should be included within the cavities because this type of component "is not substantially deformed in a firing stage for obtaining the ceramic laminated structure and a pressurizing stage previous thereto, and hence the electrostatic capacitance value, the resistance value, ... provided by the chip-like electronic component can be maintained substantially according to design." Takagi et al., col. 3, lines 12-19. That is, Takagi et al. teaches that laminated ceramic capacitors should be used to withstand the rigors of the substrate formation, which include subjecting the components to extreme heat and pressure.

In stark contrast, the capacitive structures of Klee et al. are designed to be surface-mount capacitors with a small thickness. See, e.g., col. 1, lines 62-65 of Klee et al. Moreover, it is a stated goal of this patent to fabricate its capacitive structures on "a cost-effective glass substrate." Klee et al., col. 2, lines 12-15. Accordingly, the thin, glass-based capacitive structures of Klee et al. are intended for careful placement on the surface of a circuit board, NOT to be used in

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cavities of ceramic substrates which are to be subjected to extreme heat and pressure.

As such, one of ordinary skill in the art would have been taught away from attempting to combine the Klee et al. capacitive structures with the Takagi et al. substrate as the Examiner proposes. Thus, the rejection of Claim 29 based upon these references should be withdrawn. To find otherwise would require the impermissible use of the Applicants' teachings in hindsight as a road map or template to piece together the prior art.

B. Klee et al. and Alexander

Alexander is directed to a method of producing an LTCC monolithic structure having one or more electronic components integrated therein. The method includes providing a green electronic component, providing a stack of green LTCC dielectric tape having an opening formed in the stack for receiving the green electronic component, placing the green electronic component in the opening in the stack to form a structure, and laminating and firing the structure to provide the monolithic electronic structure. See, e.g., abstract of Alexander.

While the Examiner correctly acknowledges that Klee et al. fails to teach or fairly suggest an electronic module, a capacitive structure embedded in an LTCC substrate, or an electronic device mounted on the LTCC substrate, he contends that Alexander provides these noted deficiencies. Here again, it is respectfully submitted that the prior art teaches away from such

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a selective combination. More particularly, Alexander teaches that an unfinished electronic device formed with "green" LTCC tape layers should be placed within a cavity formed in green LTCC substrate tape layers. Alexander further teaches that lamination of the substrate removes gaps or openings in the structure, and that this lamination is performed under "severe" conditions of about 70°C at 3000 psi. See, e.g., col. 5, lines 10-22 of Alexander.

As with Takagi et al., one of ordinary skill in the art would therefore have been taught away from attempting to incorporate the thin, glass-based capacitive structure of Klee et al. (which again are intended for careful placement on the surface of a circuit board, for example), in a cavity of a green substrate which is subjected to extreme heat and pressure and expands to compress the structure. That is, the Klee et al. structure is clearly not intended for the extreme heat and pressure required by Takagi et al. and Klee et al., and one of ordinary skill in the art would thus have been taught away from attempting to do so. The rejection of Claim 29 based upon Klee et al. in view of Alexander should therefore be withdrawn as well, as to find otherwise would again require the impermissible use of the Applicants' teachings in hindsight as a road map or template to piece together the prior art.

Accordingly, it is submitted that independent Claim 29 is patentable over the prior art. Its respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further

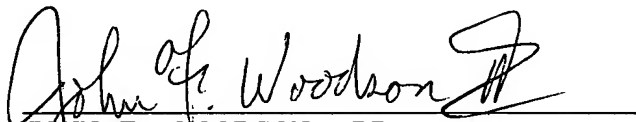
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discussion herein.

**CONCLUSIONS**

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

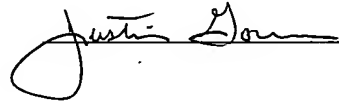


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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 26<sup>th</sup> day of January, 2005.

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